Environmental Stress Testing of Power Transistors Encapsulated in Plastic Packages

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Abstract

Power HEXFET transistors encapsulated in TO-220-style and SOT223-style plastic packages were subjected to preconditioning per the JEDEC JESD22-A113 standard, which includes solder reflow simulation and flux application, and to environmental stress testing: highly accelerated biased temperature and humidity test (HAST) and multiple temperature cycling. Electrical measurements and C-SAM mode acoustic microscopy were performed after each of the stress tests. Thermo-mechanical and moisture characteristics of the molding compounds used have been analyzed to explain the origin and evolution of the observed delaminations. An anomalous increase in leakage currents was detected after preconditioning and was explained by flux penetration to the die surface through delaminated areas between the molding compound and the die/lead-frame assembly. Different modes of parametric degradation and failures of HEXFETs observed after HAST performed in two laboratories, where different types of fluxes were used for preconditioning, confirm that flux application might have a significant effect on the results of reliability testing. The role of delaminations in the reliability of power transistors, mechanisms of moisture-induced charge instability in HEXFETs, reproducibility of HAST, and the necessity to revise the JESD22-A113 standard regarding flux application are discussed.

Key words: HEXFET, reliability, delaminations, HAST, flux, preconditioning.

1. Introduction

Delaminations between the molding compound, MC, and die or lead-frame of plastic encapsulated microcircuits, PEMs, are commonly considered as defects affecting reliability of the parts. Top-of-die (TOD) and finger-tip-of-lead (FTL) delaminations are believed to be critical due to possible wire-bond failures caused by temperature cycling [1] and/or thermal shock during solder reflow of PEMs [2]. For this reason, inspection of PEMs using acoustic microscopy (AM) is often considered as a necessary screening procedure to eliminate potential failures. However, for PEMs generally, and for power devices in plastics packages in particular, there are no sufficient data on correlation between the size and/or location of delaminations and the probability of failures. This impedes the development of justified rejection criteria during screening. Also, evolution of delaminations during environmental stress testing, and in particular, solder reflow, temperature cycling, and humidity testing, has not been investigated or understood adequately.

Another possible mechanism of failures related to delaminations is due to compromised mechanical integrity of devices in plastic packages. Delaminations might facilitate penetration of moisture and contaminations to the die surface and accelerate failures in humid environments. Failures during a highly accelerated temperature and humidity stress test (HAST) which is commonly performed at 130 ^{o}C and 85% RH, might be caused by excessive leakage currents [3], corrosion of aluminum metallization [4, 5], passivation cracks [6], and mechanical damage to wire bonds caused by moisture-induced swelling of MC [7]. The presence of delaminatoions significantly accelerates these package-related failures. Traditionally, corrosion was considered as a major moisture-related failure mechanism; however, due to dramatic improvements in the quality of molding compounds, it is not a prime cause of failures during HAST even on samples with excessive delaminations [8]. There are also reports that die-related degradation mechanisms in microcircuits, including hot carrier degradation and negative-bias-temperature-instability (NBTI) can be accelerated by moisture [9, 10]. This indicates the possibility of failures of plastic encapsulated power MOS devices operating in humid environments by a moisture-induced charge instability mechanism.

This study was initiated as a follow-up investigation of AM and HAST failures revealed

during screening and qualification testing of commercial power transistors for space applications. Thermo-mechanical and moisture characteristics of MCs used have been analyzed to explain the origin and development of delaminations during environmental stress testing. Experimental data indicated significant changes in delaminations as a result of these testing and the possibility of flux penetration to the die surface through delaminated areas in TO-220-style packages. The effect of HAST on characteristics of power transistors has been studied to better understand the mechanism of parametric degradation in humid environments. Delaminations in devices encapsulated in TO-220-style packages and ambiguous requirements of JEDEC JESD22-A113 standard regarding flux application prior to reliability testing of surface mount devices are believed to contribute to poor reproducibility of HAST.

2. Results of screening and qualification testing

Five types of power HEXFETs (2680 pcs.) manufactured by the same manufacturer in TO-220- and SOT-223-style plastic packages were screened using C-SAM-mode acoustic microscopy. The proportion of rejects due to delaminations varied from 2.3% to 28%. Acoustic microscopy revealed delaminations at paddle, TOD and FTL areas of the devices. Fig. 1 shows an example of these delaminations; X-ray images are provided to better understand internal features of the design and location of delaminations. Note that devices in SOT-223 packages had no TOD delaminations.

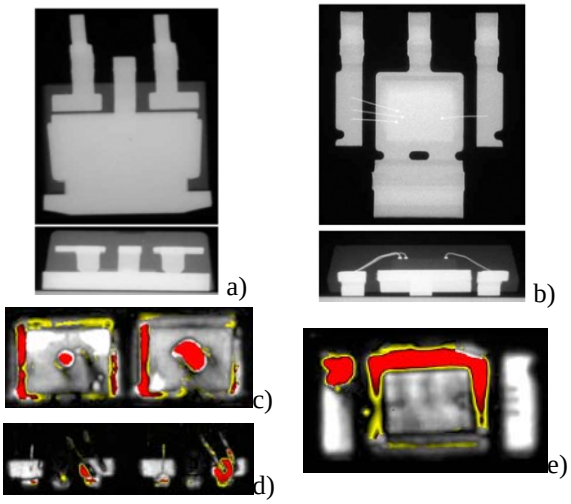

Fig.1. X-ray views (a, b) and typical delaminations observed in HEXFETs encapsulated in TO-220-style (c, d) and SOT-223-style (e) packages.

Five types of power HEXFETs with 30 samples in each lot were subjected to HAST as a part of reliability qualification testing. Following preconditioning per the JEDEC JESD22-A113 standard, the parts were tested at 130 ^{o}C and 85% relative humidity for 250 hrs. under bias conditions.

Electrical measurements after testing showed that 4 out of 5 lots had failures varying from 27% to 97%. Most of the failures were due to increased leakage currents and decreased drain-source breakdown voltages. Internal examinations revealed sites of local corrosion on the surface of aluminum metallization similar to shown in Fig. 2; however, no correlation between corrosion and failure sites were found and a significant proportion of failures was due to parametric degradation of the transistors.

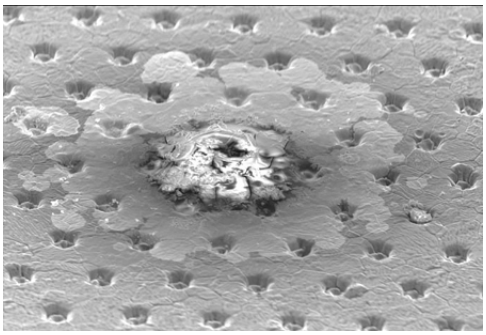

Fig. 2. An example of local corrosion on the surface of Al metallization. X-ray microanalysis indicated the presence of chlorine contamination in corrosion product. (Picture courtesy of C. Greenwell)

Fig. 3 shows typical transfer I-V characteristics of several failed parts and one reference part. The curves indicate the presence of a hump at negative VGS voltages, which is several orders of magnitude greater for failed parts than for a reference part. The threshold voltages decreased from ~1.75 V for normal parts to +0.5 to –0.5 V for failed parts, thus suggesting an increase of positive charge at the gate oxide/silicon interface. This VTH shift might open transistors even at VGS = 0 V, which explains excessive drain leakage currents observed on many HAST failures.

Note also that AM after HAST testing revealed excessive TOD delaminations in most of the parts encapsulated in TO-220 style packages, whereas no delaminations of this type were observed in SOT-223 packages.

3. Experiment

Environmental stress testing was performed on three types of power n-channel HEXFETs: two types in TO-220-style packages (referred in the following as FET1 and FET2) and one type in SOT-223-style package (FET3).

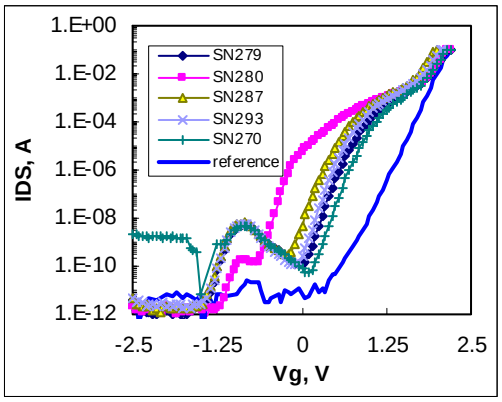

Fig. 3. Transfer characteristics of several HAST failures (marks) and of a normal part (line).

3.1. Temperature cycling

To evaluate thermo-mechanical robustness of the parts with delaminations, 30 worst-case delamination samples of each part type were electrically tested, environmentally stressed, and examined using acoustic microscopy. Electrical measurements and C-SAM-mode AM examinations were carried out before testing; after soldering reflow simulation (preconditioning per JEDEC JESD22-A113); after 100, 300, and 1000 temperature cycles (TC) between –55 and +125 ^{o}C (condition TC0); after 100 and 300 cycles between 0 and 180 ^{o}C (condition TC1); and after 100 and 300 cycles between 20 and 200 ^{o}C (condition TC2). Note that all TC were performed with the same temperature swing but at different Tmax to address the issues related to the validity of TC testing at temperatures exceeding the glass transition temperature (Tg) of molding compound.

3.2. HAST

The original HAST during reliability qualification of the transistors was performed at dynamic electrical conditions (in the following referred as condition HAST-A): VDS = 90 V, VGS = 10 V, f = 500 Hz, duty cycle 10%, limiting resistors (RL) at the gate and drain 10 kOhm. To investigate what conditions (drain or gate bias) are responsible for the observed parametric shifts in transistors, two static bias conditions were used for testing: condition HAST-B: VDS = 90 V, RL = 10 kOhm, VGS = 0 V and condition HAST-C: VDS = 0 V, VGS = 10 V, RL = 10 kOhm.

For comparison, to evaluate the effect of moisture, high temperature bias (HTB) testing at conditions A, B, and C were performed at 130 ^{o}C in a regular temperature chamber. All parts before HAST and HTB testing were preconditioned per the JEDEC JESD22-A113 standard.

To avoid possible charge redistribution, electrical measurements, which were performed periodically through the testing, were carried out on devices cooled to room temperature with applied voltages. Each group of transistors had five parts minimum. All electrical measurements were performed using an HP4156A semiconductor parameter analyzer.

4. Test results

4.1. Effect of preconditioning and temperature cycling

A fraction of delamination was estimated for every device as a ratio of the delaminated area to the whole surface area for the three major elements of the device: die surface, paddle, and internal section of the leads. All AM data analyzed were top-side C-SAM images of the devices. Evolution of average values of the calculated ratios for the three part types are displayed in Fig. 4.

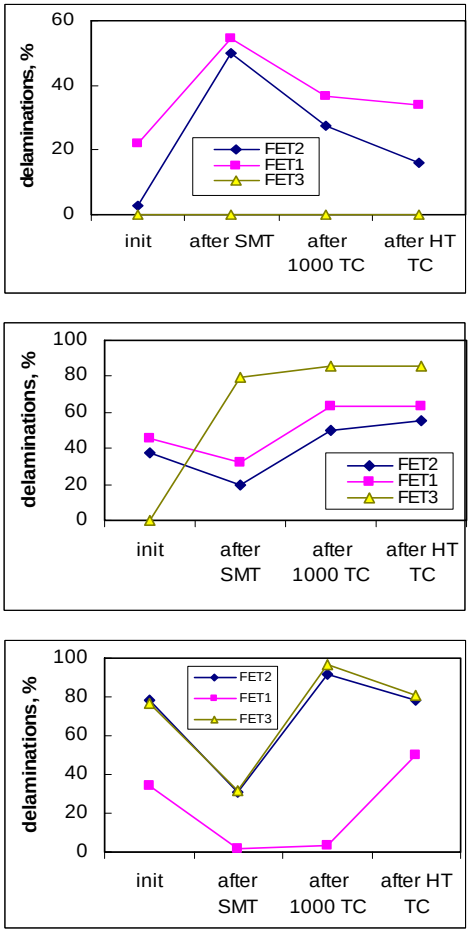

Fig. 4. Evolution of delaminations at top-of-die (a), leads-to-MC (b), and paddle-to-MC (c).

The results show that thermal stresses during soldering reflow and temperature cycling changes

delaminated areas substantially and depending on the level of stress, previous conditions, and package style, the proportion of delamination might increase or decrease. Both parts in TO-220-style packages manifested similar variations; however, evolution of delaminations for devices in SOT-223 packages was different. SOT-223 packages had no TOD delaminations throughout the environmental stress testing, whereas for TO-220-style packages the proportion of TOD delaminations rose to ~50% after SMT simulations. For SOT-223 devices the leads-to-MC delaminations increased from 0 to 80% after soldering reflow simulation, but for TO-220-style devices it decreased from ~40% to ~25%.

In spite of the presence of delaminations, no failures or any substantial parametric variations in the parts were observed during temperature cycle testing. However, FET1/2 parts manifested a significant increase in drain (IDS) and gate (IG) leakage currents after SMT simulation (preconditioning). Fig. 5 shows evolution of gate currents during environmental stress testing for three part types.

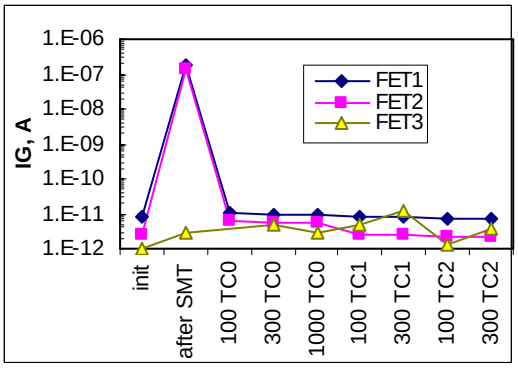

Fig. 5. Evolution of gate currents during thermal stress testing.

Note that the leakage currents for FET3 devices were in the picoampere range and had no anomalies during this testing. Also, the increase in IG for FET1/2 devices, which exceeded 4 orders of magnitude, cleared during the following measurements. The reason for this anomaly will be discussed in section 5.3.

4.2. Degradation of characteristics after HAST

Variations of average VTH and IDS values for FET1 HEXETs during HAST and HTB testing are shown in Fig. 6.

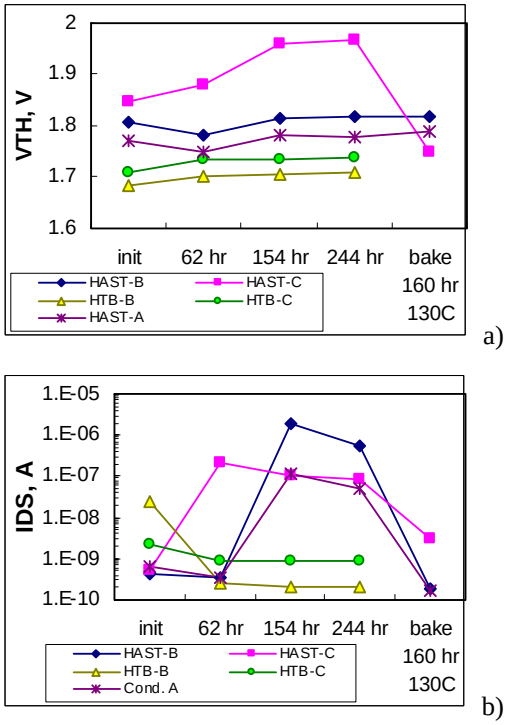

Fig. 6. Average VTH (a) and IDS (b) variation with time during HAST and HTB testing.

The results for dynamic HAST-A conditions were close to the results of static HAST-B, conditions. Testing at the HAST-C condition resulted in some increase in VTH, and all HAST conditions caused raising of IDS by 3 to 4 orders of magnitude. No significant variations were observed during HTB testing, thus suggesting that the observed variations were due to the presence of moisture. Baking at 130 ^{o}C after HAST mostly recovered characteristics of the devices.

Although both static conditions, HAST-B and HAST-C, resulted in an increase of IDS, the drain-source IV characteristics for these groups were different (see Fig. 7). At low voltages, HAST-C resulted in significant increase of IDS, which remained stable at VDS > 1 V. Contrary to that, HAST-B resulted in a linear increase of IDS in double logarithmic coordinates, thus indicating that a power law controls IDS variations at VDS > 1 V. Baking at 130 ^{o}C for 160 hrs reduced the currents by several orders of magnitude. Testing at the HTB-C condition resulted in a similar shape of I-V curves as HAST-C, but the increase of IDS was approximately 3 orders of magnitude less.

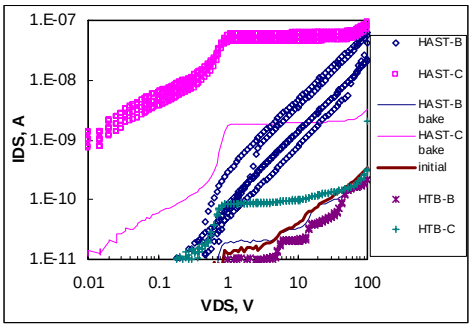

Fig. 7. Output characteristics at VGS = 0 of several HEXFETs after different conditions of HAST and HTB testing.

Transfer characteristics of the parts before and after HAST and HTB testing are shown in Fig. 8. A peculiarity of these characteristics is the presence of a hump of leakage currents at negative voltages with maximum IDS at VGS below -0.7 V. The amplitude of the hump after HAST-C was more than 3 orders of magnitude larger than after HTB-B/C or HAST-B conditions, which did not change currents significantly compared to the initial characteristics. Note also that HAST-C testing resulted in substantial decrease of the slope of the IDS-VGS characteristics in the subthreshold region. This can explain an increase in VTH shown in Fig 6a. Baking at 130 ^{o}C, similar to what was shown in Fig. 6, significantly decreased hump currents and the slope.

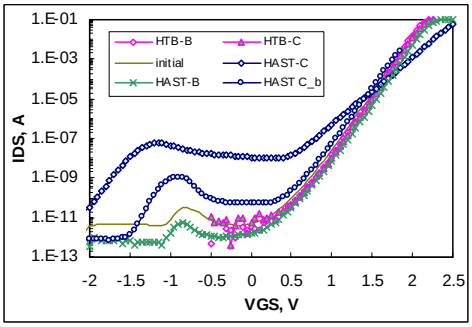

Fig. 8. Typical transfer characteristics after different conditions of HAST and HTB testing.

Our HAST results indicate no variations (HAST-A/B conditions) or a slight increase (HAST-C conditions) of VTH to less than 0.15 V. Contrary to that, HAST during reliability qualification caused a significant, up to 1.2 to 2.2 V, decrease in VTH. To evaluate the effect of possible variations in conditions during HAST, additional experiments have been carried out at 150 ^{o}C/85%RH and a gate voltage increased to 15 V for 96 hrs. However, no significant variations in VTH were observed. A possible reason of poor reproducibility of HAST testing is discussed below in section 5.5.

Similar to what was observed on devices failed qualification testing, our experiments also revealed excessive TOD delaminations (for TO-220-style packages) and paddle/FTL delaminations (both types of packages) after HAST.

5. Discussion

The results of testing reported in the previous section rise several questions regarding degradation mechanisms in these devices:

- Why are FET1/2 devices contrary to FET3 prone to form TOD delaminations?
- What is the significance of delamiantions for reliability of the parts?
- What is the mechanism of moisture-induced parametric degradation?
- What is the origin of anomalous leakage currents after SMT simulation?
- Why was significant degradation in the threshold voltages observed after qualification HAST testing not reproduced in our experiments?

The discussion below is an attempt to answer these questions.

5.1. The origin and evolution of delaminations

Transistors in TO-220-style packages (FET1/2) contrary to devices in SOT-223 packages (FET3) had had initially up to 20% of TOD delaminations, which increased further after soldering reflow simulation and HAST. To better understand the origin and evolution of these delaminations, thermo-mechanical and moisture characteristics of the molding compounds used have been analyzed.

The glass transition temperature and coefficients of thermal expansion in the glassy (CTE1) and rubbery (CTE2) states of MCs were measured using a thermal mechanical analyzer, TMA2940, manufactured by TA Instruments. The coefficient of moisture expansion (CME) was measured using a liquid dilatometry technique described in [11].

Results of thermo-mechanical measurements before and after HAST are shown in Table 1. Characteristics of MCs used for FET1 and FET2 were similar and featured a relatively high CTE1, which did not change significantly after HAST (CTE data after HAST are not shown in the table). Moisture sorption in the HAST chamber resulted in ~10 ^{o}C decrease of Tg. The use of MC with a relatively high CTE1 for FET1/2 probably can be explained by the necessity to match the CTE of MC with aluminum wires (~24 ppm/^{o}C), which are used in these devices to interconnect the die and the leads. A decrease in Tg due to moisture sorption is common for molding compounds and is due to the plasticizing effect of absorbed moisture [12].

Table 1. Thermo-mechanical characteristics of molding compounds.

	Tg, °C	CTE1, ppm/°C	CTE2, ppm/°C	Tg, °C HAST
FET1	169	22	67	157
FET2	165	22	66	-
FET3	153	16	60	154

Moisture characteristics of MCs including moisture sorption (dM/Mo) swelling (dV/Vo) and CME after HAST at 130 and 150 °C are shown in Table 2. Considering that CME values might vary from 0.2 to 0.5 [7, 11], the presented data are within the range of characteristics, which are typical for orto-cresol novolac MCs used for plastic encapsulation of microcircuits.

Table 2. Moisture characteristics of molding compounds.

	HAST 130 °C			HAST 150 °C		
	dM/M_o %	dV/V_o, %	CME, %/%	dM/M_o %	dV/V_o, %	CME, %/%
FET1	0.55	0.51	0.31	0.85	0.87	0.34
FET3	0.34	0.39	0.38	0.32	0.32	0.33

Relatively large Tg and CTE1 values for FET1/2 devices and asymmetry in the location of MC relative to the lead-frame are likely accounted for substantial mechanical stresses formed in MCs after curing and cooling of the devices to room temperature. These stresses warp the package facilitating formation of initial TOD delaminations. Exposure of the parts to high temperatures during solder reflow simulation results in significant expansion of MC and, due to a relatively thick and rigid copper paddle, to warping of the package and formation of delamination as it is schematically shown in Fig. 9. After soldering, the MC shrinks; however, due to the creep at high temperatures, cooling does not restore the original conditions in the package, resulting in some remnant TOD delaminations.

Transistors FET1/2, contrary to FET3, had no passivation above the aluminum metallization on the surface of the die. Because the adhesion of MCs depends on the material of the substrate [13] and is normally optimized to dies passivated with a glass layer, it is possible that adhesion to aluminum metallization is relatively weak. This would enhance the trend of formation of delaminations of transistors in TO-220 packages compared to devices in SOT-223 packages.

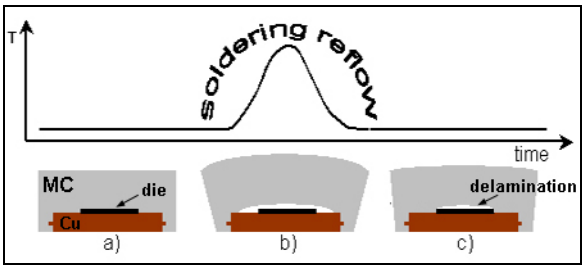

Fig. 9. Schematic showing deformation of TO-220-style package during solder reflow.

Moisture-induced swelling of MCs in the HAST chamber also causes extensive deformations of MC, which can be estimated as Δ = CME×dM/Mo. Considering data in Tables 1 and 2, this expansion would be equivalent to a temperature increase of $\delta T = \Delta/CTE1 = 78$ °C. At a temperature of HAST of 130 °C, this would result in deformations similar to the thermal deformations at 208 °C, which is close to the temperature of reflow soldering, and together with moisture-facilitated creep would cause similar increase in TOD delaminations.

5.2. Moisture-induced parametric degradation

The hump on IDS curves at negative VGS voltages on parts that failed qualification testing (Fig. 3) and to a larger degree on devices after HAST-C testing (Fig. 8) is similar to what is known for the gate-controlled P^+-N diodes and can be explained by a surface electron-hole generation of charge carriers in a depletion area of silicon under the gate [14]. According to this mechanism, the excessive leakage currents in n-channel HEXFETs at VGS < 0 V depend on the concentration of fast surface states at the Si/SiO_2 interface. Fig. 10. shows an overall view of the die and explains the design of a HEXFET cell.

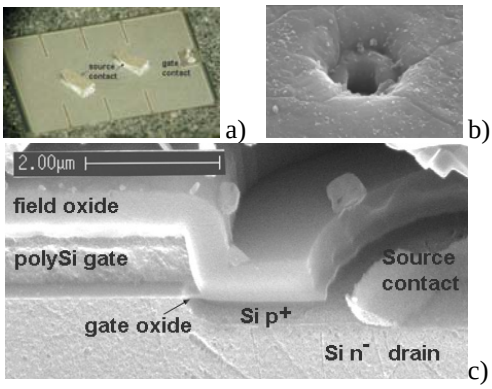

Fig. 10. An overall view of the die (a), SEM view showing grain boundaries in aluminum metallization (b), and a cross section of a cell (c).

Fig. 11 shows a schematic of the transistor at different conditions under the gate. An increase in the drain voltage expands the depletion area

according to the power law, ~ $VDS^{0.5}$, and raises the leakage current due to extended volume where charge carriers are generated via generation-recombination centers in the bulk of silicon. However, when the concentration of surface states is great enough, the rate of bulk generation is much smaller compared to the surface generation and the total leakage current, which is a sum of bulk and surface components, is virtually independent of VDS. This explains stability of the drain currents at VDS > 1 V after HAST-C testing (Fig.7).

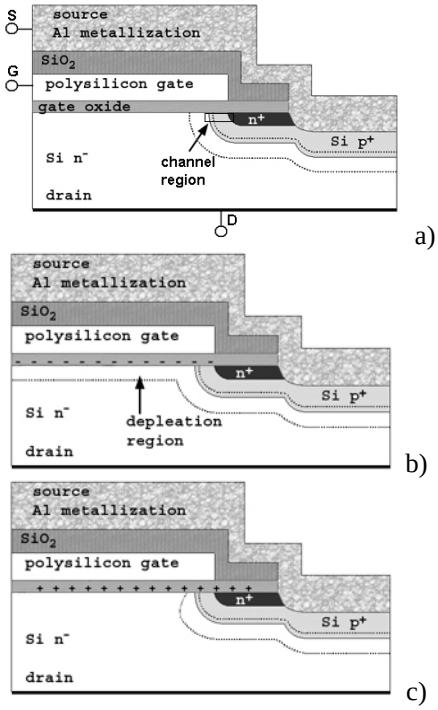

Fig. 11. Schematic of a HEXFET cell at no charge (a), depletion (b) and accumulation (c) conditions in the gate oxide.

A decrease of the slope in the subthreshold region after HAST-C testing (Fig. 8) is in agreement with the increase of IDS at VGS < -0.7 V and indicates extensive generation of the surface states at the Si/SiO_2 interface not only along the periphery of the polysilicon gate, but also at the channel region. The fact that no increase in the hump was observed after HTB testing indicates that the process of surface states generation is induced by the presence of moisture in the gate oxide. This process is probably similar to the moisture-induced high temperature bias degradation observed in [9].

A gradual increase of drain currents with the gate voltages after HAST-B testing (see Fig. 7) indicates a soft surface breakdown and suggests a formation of positive charges at the gate-drain interface as it is schematically shown in Fig 11c. At HAST-B, electrical bias creates a strong electrical field in the gate oxide, which is directed from the silicon to the gate (VGS = 0, VDS = 90 V). This condition is equivalent to a negative bias at the gate relative to silicon and might generate positive charges in the oxide of MOSFETs via a mechanism similar to the NBTI in MOS devices, which is also activated by the presence of moisture [10].

For moisture to access the gate oxide in FET1/2 devices, it should penetrate through a layer of MC, aluminum metallization of the source contact, and CVD field oxide. A characteristic time of moisture diffusion through a layer of a thickness h with the diffusion coefficient D can be estimated as h^2/D. At a thickness of MC h = 3.2 mm and D at 130 ^oC ~ $(1.5\text{-}3)\times10^{-11}$ m^2/s [15], the time for moisture diffusion would be 90 to 180 hrs. According to Fig. 6, degradation of IDS was observed already after 62 hrs. This indicates that for TO-220 packages, moisture ingress occurs most likely through gaps and delaminations between the leads and the molding compound.

At a thickness of the field CVD silicon oxide layer of ~1 μm and the diffusion coefficient at 130 ^oC of ~ 5×10^{-17} m^2/s [16], the characteristic time of diffusion through the oxide is ~3 hrs only. Pores in the field oxide (see Fig. 12a) would further reduce the time for moisture to reach the gate oxide.

Considering that source metallization covers most of the die surface (see Fig. 10a.) and that aluminum is non-permissive to moisture, no water molecules should have reached the gate oxide of the transistors. However, the presence of the grain boundaries, and microcracks in aluminum metallization similar to those shown in Fig. 10b and 12b, might create a diffusion path allowing water molecules to penetrate to the gate oxide (most likely along the surface of the polysilicon gate). Application of nitride passivation, which is considered a major barrier against moisture penetration in plastic encapsulated microcircuits, would probably significantly reduce moisture related degradation in these devices.

5.3. Anomalous leakage currents after preconditioning

To understand the behavior of anomalous leakage currents observed after preconditioning (see Fig. 5), a group of six FET1 devices was conditioned per JEDEC JESD22-A113, which included soaking in a humidity chamber at 85^oC/85%RH for 160 hrs., running three times through a solder reflow chamber, applying flux by immersing into a water-soluble flux, rinsing in deionized water, and blowing with air. After preconditioning, the parts were baked at 125 ^oC, then stored at room temperature and 100% RH for

15 hours in an attempt to cause water condensation on the internal elements of the parts, and finally immersed in water for 10 seconds. Results of electrical measurements during these testing are shown in Fig. 13a. Similar to what was observed before, preconditioning has increased leakage currents by 3 to 5 orders of magnitude. Baking at 125 ^{o}C for 1 hr. decreased the currents substantially. In four parts, additional baking for 3 hrs. virtually restored the initial level of the currents, and in two parts, it remained approximately 10 times larger than before preconditioning.

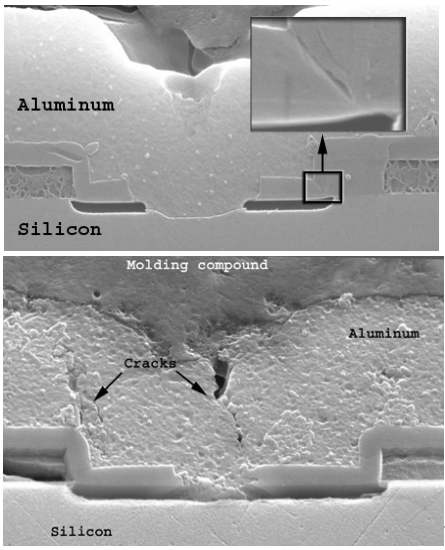

Fig. 12. Cross sections of a HEXFET cell showing micropores in the field oxide (a) and microcracks in the source aluminum metallization (b).

These results indicate that anomalous leakage currents are due to penetration of flux to the unpassivated die surface and bridging gate and source metallizations. The most probable path for flux to reach the die surface is along the delaminated interface between the MC and the central lead connected to the paddle. During baking, the flux dries out and the currents return to their initial values. It is interesting that storing in high humidity conditions and even immersing in water did not increase leakage currents. This fact is probably due to a better wettability of the flux compared to water, which allows flux penetration even through tiny gaps in the package.

During additional experiments with a separate group of devices, characteristics of the parts were monitored after flux application for several days (see Fig. 13b). The data suggest that excessive leakage currents are caused by flux application even on devices stored for several days after solder reflow simulation and that at room temperature drying of the flux trapped inside packages might take more than 3 to 4 days.

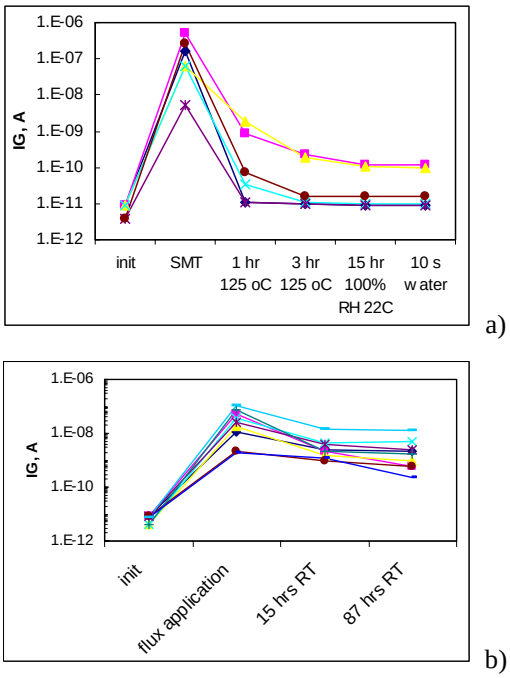

Fig. 13. Evolution of excessive leakage currents caused by flux application. The effects of bake, humidity, and moisture (a). Storing at room temperature (b).

One might expect that larger TOD delaminations would enhance the access of flux and respectively result in higher leakage currents. An attempt has been made to correlate the level of leakage currents after flux application and the proportion of the delaminations at the die surface measured by CSAM-mode AM. In Fig. 14 the leakage currents after SMT simulation are plotted against the proportion of TOD delaminations. The fact that no correlation was observed, suggests that C-SAM examination are not effective to screen out potential electrical failures in a lot prone to form excessive delaminations.

5.4. The effect of delaminations on results of temperature cycling

In spite of excessive delaminations at critical wire-bond areas of the devices, no failures were observed during soldering reflow simulations and multiple temperature cycling. For FET3 transistors, which were bonded with gold wires and had FTL delaminations, this result is similar to what was observed earlier during testing of PEMs in SOIC-8 style packages, where no wire-bond failures were detected during TC of devices rejected by acoustic microscopy [17]. This indicates that secondary bonds in PEMs, which typically interconnect gold

wires with silver-plated copper lead-frame, are strong enough and can provide reliable connection even in the presence of delaminations.

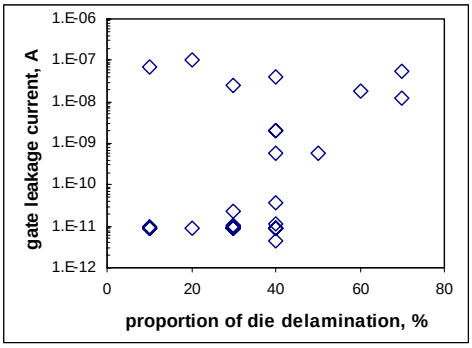

Fig. 14. Correlation between the flux-induced leakage currents and proportion of TOD delaminations.

Wire bonds in HEXFET devices in TO-220-style packages, in spite of extensive TOD delaminations, also survived thermal shocks during SMT simulation and multiple temperature cycling. The possibility of wire bond failures during environmental stress testing of devices with TOD delaminations is due to more freedom for MCs to shift at delaminated areas, especially at the corners of the die [2, 6, 18, 19]. In our case, interconnection in FET1/2 devices was made with large-diameter (~150 and 250 μm) aluminum wires, which have a high breaking strength and elongation. This, together with a central location of wires connected to the source on the die surface where the stresses are minimal, probably allowed the devices to withstand environmental stress testing without failures.

Note that no failures were observed even after temperature cycling at maximum temperatures of 180 and 200 ^{o}C, which 11 to 47 ^{o}C exceeded the glass transition temperature of molding compounds used (see Table 1). This confirms that Tg is not a major factor affecting results of temperature cycle testing of PEMs [20].

5.5. Preconditioning and reproducibility of HAST

The results of HAST indicate that moisture can penetrate to the gate oxide in HEXFET devices; however, the level of degradation caused by the moisture-induced charge instability mechanism in our experiments was much less than the one revealed during qualification reliability testing. A significant VTH degradation in the latter case is most likely due to alkali contaminations, which penetrated to the die surface through delaminations between the MC and lead frame. The effect of cleanliness of the test system (surface of packages, sockets, and boards used during HAST) on results of HAST of memory microcircuits has been shown in [21]. Considering that sodium ions can penetrate through passivation and grain boundaries in Al metallization [22], and that their concentration in flux might be high, external contamination (on the package due to flux application and/or in the system used for HAST) was most likely the major reason for failures of transistors during reliability qualification testing.

It should be noted also that contaminations might penetrate to the die surface in a HAST chamber even if packages did not have any delaminations before the testing. Moisture-induced decrease of adhesion, swelling, and deformation of a package under HAST conditions might cause delaminations and create a free path for external contaminations to reach the die surface. The probability of such delamination to occur is especially significant for devices encapsulated in MCs with relatively low glass transition temperatures and high CME [20].

Preconditioning of nonhermetic surface-mount devices prior to long-term reliability testing per JESD22-A113D is performed to simulate the impact of solder reflow. The preconditioning sequence includes application of activated water-soluble flux to the device leads by bulk immersion of the entire parts in flux at room ambient for 10 seconds minimum after reflow solder cycles are completed. However, no specific requirements for the flux regarding the presence of contaminations and wettability are given, which potentially creates ambiguity in the reliability test results. Currently, dozens of various types of fluxes with different corrosivity and content of ionic chemicals are used in electronics. Obviously, application of different fluxes, even within a water-soluble group of fluxes, in different laboratories might result in different failure rates during HAST.

Flux application is an uncontrollable source of contamination, which affects more severely devices with delaminations where there is a direct path for contaminations to reach the die surface. The difference in the fluxes used, and, in particular, the difference in the concentration of alkali ions, might be accounted for poor reproducibility of HAST results in our experiments and during reliability qualification testing.

Typically, activated fluxes, which are required per JESD22-A113D, are much more aggressive and have more contaminations compared to mildly activated or no clean fluxes. Activated fluxes promote corrosion, might adversely affect electrical characteristics of devices, and are rarely used for assembly of boards intended for high-reliability applications. Besides, solder pastes used for surface mount technology contain typically mildly activated

fluxes and normally devices never contact activated fluxes.

The use of activated fluxes and the method of their application mean that the JEDEC JESD22-A113D standard exercises worst case conditions regarding possible contamination of the parts during the assembly process. For high-quality products, when adequate material and process control is used, these conditions most likely would never occur. This means, that during the reliability testing the recommended preconditioning might result in failures that would never happen in real applications. Unfortunately, in most cases, when a failure during qualification testing occurs, it is extremely difficult to find a root cause of the failure and/or relate failures to the flux immersion. For high reliability applications this would mislead or significantly complicate analysis of the risk related to using parts from the failed lot.

To assure that that the condition of the parts used for reliability testing is similar to real applications, and to provide better reproducibility of test results, preconditioning should be adequate to real-life assembly conditions. However, for the cases in which parts are expected to be exposed to extreme environments, including severe contamination during assembly and/or operation, the current standard might be suitable provided that the necessary characteristics of flux are specified.

6. Conclusions

- Acoustic microscopy measurements revealed multiple delaminations at critical wire-bond areas in power HEXFET devices in TO-220- and SOT-223-style packages. Transistors in TO-220-style packages, contrary to devices in SOT-223 packages, had TOD delaminations, which significantly increased after solder reflow simulation and HAST. The tendency of devices in TO-220-style packages to form TOD delaminations was related to the specifics of their design and to high CTE and CME values of the molding compound used.

- In spite of the presence of delaminations, no wire bond failures or any substantial parametric variations in the parts were observed during solder reflow thermal shock and 1000 TC from –55 to +125 ^{o}C. This indicates that wire bonds in PEMs might be strong enough to provide reliable interconnection even in the presence of delaminations. The parts also withstood without failures 600 additional TC at temperatures exceeding the glass transition temperature of MC.

- A significant increase, up to 5 orders of magnitude, in leakage currents was observed in HEXFETs encapsulated in TO-220-style packages after preconditioning per the JESD22-A113D standard. This anomaly was due to high wettability of flux allowing its penetration to the surface of die through delaminations between the MC and lead-frame and bridging the gate and source metallizatoion. No correlation between the flux-induced leakage currents and proportion of delaminations were observed.

- The results of HAST and HTB testing indicated that moisture can penetrate to the gate oxide in HEXFET devices through the grain boundaries and microcracks of aluminum metallization and micropores in the field oxide and cause parametric degradation via generation of surface states at the gate oxide/silicon interface. A significant decrease in the threshold voltage after reliability qualification HAST suggests that alkali ions also can penetrate to the gate oxide, causing degradation by a mobile ionic charge instability mechanism.

- The difference in fluxes used for preconditioning prior to reliability testing in different test laboratories might be accounted for poor reproducibility of HAST. Application of water-soluble activated fluxes per the JEDEC JESD22-A113D standard might cause contamination of the devices to a level they would never experience during assembly of cards intended for high-reliability applications. This might cause failures, which would never happen provided that adequate preconditioning is performed, and mislead the assessment of the risk of parts' application.

7. Acknowledgments

This work was sponsored by the NASA Electronic Parts and Packaging (NEPP) Program and GSFC projects. The author thanks Darryl Lakins and Ashok Sharma from GSFC for support of this work, as well as Chris Greenwell and Gerry Kiernan from QSS Group, Inc., and Bruce Meinhold from Jackson and Tull for providing samples and information on failure analysis and reliability test results. The author also would like to acknowledge Jeanne Ilg for editing of this manuscript.

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